EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	2	("5008671").PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/03/30 10:51
L2	654	(341/133,134,135,136144,153).CCLS.	USPAT	OR	OFF	2006/03/30 10:51
L3	2144	(341/133,134,135,136,144,153).CCLS.	USPAT	OR	OFF	2006/03/30 10:51
L4	242	(341/144).CCLS.	US-PGPUB	OR	OFF	2006/03/30 10:52
L5	587	unit cell digital analog	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/03/30 10:52
L6	8	unit cell digital analog and l4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/03/30 10:54
L7	0	make unit cell digital analog and l4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/03/30 10:55
L8	0	make unit cell digital analog and l3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/03/30 10:55
L9	5	make cell digital analog and l3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/03/30 10:55

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1. **A dynamically controlled and refreshed low-power level-up shifter**
Zhengrong Huang; Savaria, Y.; Sawan, M.;
Circuits and Systems, 2004. MWSCAS '04. The 2004 47th Midwest Symposiur
Volume 1, 25-28 July 2004 Page(s):I - 97-100 vol.1
Digital Object Identifier 10.1109/MWSCAS.2004.1353906
AbstractPlus | Full Text: PDF(483 KB) **IEEE CNF**
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2. **Robust design of a dynamically controlled low-power level-up shifter ope V**
Zhengrong Huang; Savaria, Y.; Sawan, M.;
Circuits and Systems, 2004. NEWCAS 2004. The 2nd Annual IEEE Northeast
20-23 June 2004 Page(s):321 - 324
Digital Object Identifier 10.1109/NEWCAS.2004.1359096
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3. **Automatic Test Equipment in the Production Process**
Boudreault, A.;
Manufacturing Technology, IEEE Transactions on
Volume 4, Issue 2, Dec 1975 Page(s):48 - 52
AbstractPlus | Full Text: PDF(728 KB) **IEEE JNL**
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4. **Picture coding using pseudo-random noise**
Roberts, L.;
Information Theory, IEEE Transactions on
Volume 8, Issue 2, Feb 1962 Page(s):145 - 154
AbstractPlus | Full Text: PDF(1984 KB) **IEEE JNL**
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5. **Exploding the Nyquist barrier misconception**
Marple, L.;
Signal Processing Magazine, IEEE
Volume 13, Issue 5, Sept. 1996 Page(s):32, 34, 36, 38, 40, 42
Digital Object Identifier 10.1109/79.536827
AbstractPlus | Full Text: PDF(1592 KB) **IEEE JNL**

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6. **Using distributed objects to build the Stanford digital library Infobus**
Paepcke, A.; Baldonado, M.Q.W.; Chang, C.-C.K.; Cousins, S.; Garcia-Molina,
Computer
Volume 32, Issue 2, Feb. 1999 Page(s):80 - 87
Digital Object Identifier 10.1109/2.745724
AbstractPlus | References | Full Text: PDF(180 KB) **IEEE JNL**
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7. **An accelerated decomposition algorithm for robust support vector Machi**
Hu, W.J.; Song, Q.;
Circuits and Systems II: Express Briefs, IEEE Transactions on [see also Circui
Analog and Digital Signal Processing, IEEE Transactions on]
Volume 51, Issue 5, May 2004 Page(s):234 - 240
Digital Object Identifier 10.1109/TCSII.2004.824044
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8. **Extended Voltage Swell Ride-Through Capability for PWM Voltage-Sourc**
Burgos, R.P.; Wiechmann, E.P.;
Industrial Electronics, IEEE Transactions on
Volume 52, Issue 4, Aug. 2005 Page(s):1086 - 1098
Digital Object Identifier 10.1109/TIE.2005.851643
AbstractPlus | Full Text: PDF(744 KB) **IEEE JNL**
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9. **Peer-to-peer data preservation through storage auctions**
Cooper, B.F.; Garcia-Molina, H.;
Parallel and Distributed Systems, IEEE Transactions on
Volume 16, Issue 3, Mar 2005 Page(s):246 - 257
Digital Object Identifier 10.1109/TPDS.2005.34
AbstractPlus | Full Text: PDF(672 KB) **IEEE JNL**
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10. **Serious graphics: how a picture can make or break it**
Fox, S.;
Engineering Management Journal
Volume 15, Issue 3, June-July 2005 Page(s):47
AbstractPlus | Full Text: PDF(71 KB) **IEE JNL**

11. **Automatic Generation of Digital System Schematic Diagrams**
Arya, A.; Swaminathan, V.V.; Misra, A.; Kumar, A.;
Design Automation, 1985. 22nd Conference on
23-26 June 1985 Page(s):388 - 395
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12. **Intelligent integrated low voltage switch**
Shaohua Ma; Zhiyuan Cai; Wei Li; Jian Wang;
Power Tech Conference Proceedings, 2003 IEEE Bologna
Volume 2, 23-26 June 2003 Page(s):5 pp. Vol.2
Digital Object Identifier 10.1109/PTC.2003.1304601
AbstractPlus | Full Text: PDF(374 KB) **IEEE CNF**
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13. **Research on the Intelligence High-Voltage Circuit Breaker Based on DSP**
Shaohua Ma; Li Yu; Zhiyuan Cai; Wei Li;

Transmission and Distribution Conference and Exhibition: Asia and Pacific, 20
15-18 Aug. 2005 Page(s):1 - 5
Digital Object Identifier 10.1109/TDC.2005.1547126

AbstractPlus | Full Text: PDF(408 KB) **IEEE CNF**
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☐ **14. Non-contact interrogation of railroad axles using laser-based ultrasonic i**
Gonzates, K.; Kendarian, S.; Carter, D.; Smith, A.; Morgan, R.;
Rail Conference, 2005. Proceedings of the 2005 ASME/IEEE Joint
16-18 March 2005 Page(s):145 - 150

AbstractPlus | Full Text: PDF(396 KB) **IEEE CNF**
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☐ **15. Maintaining the integrity of XML signatures by using the manifest elemer**
Hussain, O.K.; Soh, B.;
Industrial Electronics Society, 2004. IECON 2004. 30th Annual Conference of
Volume 1, 2-6 Nov. 2004 Page(s):493 - 495 Vol. 1
Digital Object Identifier 10.1109/IECON.2004.1433358

AbstractPlus | Full Text: PDF(2273 KB) **IEEE CNF**
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☐ **16. A study of the elliptic curve cryptology applies to the next generation prc**
Po-Hsian, H.; Ching-Wei, C.;
Security Technology, 2004. 38th Annual 2004 International Carnahan Confere
11-14 Oct. 2004 Page(s):233 - 238
Digital Object Identifier 10.1109/CCST.2004.1405398

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Yeary, M.; Zhang, W.; Trelewicz, J.Q.;
Instrumentation and Measurement Technology Conference, 2004. IMTC 04. P
21st IEEE
Volume 2, 18-20 May 2004 Page(s):913 - 916 Vol.2
Digital Object Identifier 10.1109/IMTC.2004.1351211

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☐ **18. Pocket device for authentication and data integrity on Internet banking a**
de la Puente, F.; Sandoval, J.D.; Hernandez, P.;
Security Technology, 2003. Proceedings. IEEE 37th Annual 2003 Internationa
Conference on
14-16 Oct. 2003 Page(s):43 - 50
Digital Object Identifier 10.1109/CCST.2003.1297533

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☐ **19. Surface currents measured from a sequence of airborne camera images seventh working conference on current measurement technology**
Dugan, J.; Piotrowski, C.;
Current Measurement Technology, 2003. Proceedings of the IEEE/OES Seve
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13-15 March 2003 Page(s):60 - 65
Digital Object Identifier 10.1109/CCM.2003.1194284

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Allen, M.;

Cyberworlds, 2003. Proceedings. 2003 International Conference on
2003 Page(s):26 - 33
Digital Object Identifier 10.1109/CYBER.2003.1253431

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21. **Integrated programmable neurostimulator to recuperate the bladder func**
Ba, A.; Sawan, M.;
Electrical and Computer Engineering, 2003. IEEE CCECE 2003. Canadian Co
Volume 1, 4-7 May 2003 Page(s):147 - 150 vol.1
Digital Object Identifier 10.1109/CCECE.2003.1226364

AbstractPlus | Full Text: PDF(416 KB) IEEE CNF
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22. **Star tool: reengineering for Ada and C**
Boettcher, C.;
Digital Avionics Systems, 2001. DASC. The 20th Conference
Volume 1, 14-18 Oct. 2001 Page(s):4E1/1 - 4E1/10 vol.1
Digital Object Identifier 10.1109/DASC.2001.963379

AbstractPlus | Full Text: PDF(1151 KB) IEEE CNF
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23. **Re-architecting business infrastructures through global business-to-bus commerce**
Carayannis, E.G.; Alexander, J.M.;
Management of Engineering and Technology, 2001. PICMET '01. Portland Int Conference on
Volume 1, 29 July-2 Aug. 2001 Page(s):174 vol.1
Digital Object Identifier 10.1109/PICMET.2001.951899

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24. **The relative success of nanoscale RTD, SET and EQCA devices as replac CMOS at the system level**
Nikolic, K.; Forshaw, M.;
Nanotechnology, 2001. IEEE-NANO 2001. Proceedings of the 2001 1st IEEE
28-30 Oct. 2001 Page(s):272 - 276
Digital Object Identifier 10.1109/NANO.2001.966432

AbstractPlus | Full Text: PDF(337 KB) IEEE CNF
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25. **A new design for sample-rate converters**
Nagahara, M.; Yamamoto, Y.;
Decision and Control, 2000. Proceedings of the 39th IEEE Conference on
Volume 5, 2000 Page(s):4296 - 4301 vol.5
Digital Object Identifier 10.1109/CDC.2001.914577

AbstractPlus | Full Text: PDF(392 KB) IEEE CNF
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Terms used **digital make break cell** Found **3,290** of **173,942**

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Best 200 shown Relevance scale

1 Transistor placement for noncomplementary digital VLSI cell synthesis
Michael A. Riepe, Karem A. Sakallah
January 2003 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 8 Issue 1
Publisher: ACM Press
Full text available: pdf(2.97 MB) Additional Information: full citation, abstract, references, index terms

There is an increasing need in modern VLSI designs for circuits implemented in high-performance logic families such as Cascode Voltage Switch Logic (CVSL), Pass Transistor Logic (PTL), and domino CMOS. Circuits designed in these noncomplementary ratioed logic families can be highly irregular, with complex diffusion sharing and nontrivial routing. Traditional digital cell layout synthesis tools derived from the highly stylized "functional cell" style break down when confronted with such circuit t ...

Keywords: Cell Synthesis, Euler graphs, benchmark circuits, digital circuits, noncomplementary circuits, sequence pair optimization, transistor chaining, transistor placement

2 Transistor level micro-placement and routing for two-dimensional digital VLSI cell synthesis
Michael A. Riepe, Karem A. Sakallah
April 1999 **Proceedings of the 1999 international symposium on Physical design**
Publisher: ACM Press
Full text available: pdf(1.29 MB) Additional Information: full citation, references, citings, index terms

3 Laser correcting defects to create transparent routing for large area FPGA's
G. H. Chapman, Benoit Dufort
February 1997 **Proceedings of the 1997 ACM fifth international symposium on Field-programmable gate arrays**
Publisher: ACM Press
Full text available: pdf(989.88 KB) Additional Information: full citation, references, citings, index terms

4 Archival storage for digital libraries

Arturo Crespo, Hector Garcia-Molina
May 1998 **Proceedings of the third ACM conference on Digital libraries**
Publisher: ACM Press
Full text available: pdf(1.32 MB) Additional Information: full citation, references, citings, index terms

5 Users and interaction track: memex and hypertext: Icon abacus: positional display of document attributes
Eric A. Bier, Adam Perer
June 2005 **Proceedings of the 5th ACM/IEEE-CS joint conference on Digital libraries**
Publisher: ACM Press
Full text available: pdf(205.45 KB) Additional Information: full citation, abstract, references, index terms

This paper presents *icon abacus*, a space-efficient technique for displaying document attributes by automatic positioning of document icons. It displays the value of an attribute by using position on a single axis, allowing the other axis to display different metadata simultaneously The layout is stable enough to support navigation using spatial memory.

Keywords: computer-aided reading, metadata, spatial memory, visualization

6 The elements of nature: interactive and realistic techniques
Oliver Deusen, David S. Ebert, Ron Fedkiw, F. Kenton Musgrave, Przemyslaw Prusinkiewicz, Doug Roble, Jos Stam, Jerry Tessendorf
August 2004 **Proceedings of the conference on SIGGRAPH 2004 course notes GRAPH '04**
Publisher: ACM Press
Full text available: pdf(17.65 MB) Additional Information: full citation, abstract

This updated course on simulating natural phenomena will cover the latest research and production techniques for simulating most of the elements of nature. The presenters will provide movie production, interactive simulation, and research perspectives on the difficult task of photorealistic modeling, rendering, and animation of natural phenomena. The course offers a nice balance of the latest interactive graphics hardware-based simulation techniques and the latest physics-based simulation techni ...

7 Analysis of unconventional evolved electronics
Adrian Thompson, Paul Layzell
April 1999 **Communications of the ACM**, Volume 42 Issue 4
Publisher: ACM Press
Full text available: pdf(255.72 KB) html(37.68 KB) Additional Information: full citation, references, citings, index terms

8 Level set and PDE methods for computer graphics
David Breen, Ron Fedkiw, Ken Museth, Stanley Osher, Guillermo Sapiro, Ross Whitaker
August 2004 **Proceedings of the conference on SIGGRAPH 2004 course notes GRAPH '04**
Publisher: ACM Press
Full text available: pdf(17.07 MB) Additional Information: full citation, abstract

Level set methods, an important class of partial differential equation (PDE) methods, define dynamic surfaces implicitly as the level set (iso-surface) of a sampled, evolving nD function. The course begins with preparatory material that introduces the concept of using partial differential equations to solve problems in computer graphics, geometric modeling

and computer vision. This will include the structure and behavior of several different types of differential equations, e.g. the level set eq ...

9 Fault simulation of interconnect opens in digital CMOS circuits

Haluk Konuk

November 1997 **Proceedings of the 1997 IEEE/ACM international conference on Computer-aided design**

Publisher: IEEE Computer Society

Full text available: pdf(274.18 KB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

We describe a highly accurate but efficient fault simulator for interconnect opens, based on characterizing the standard cell library with SPICE; using transistor charge equations for the site of the open; using logic simulation for the rest of the circuit; taking four different factors, that can affect the voltage of an open, into account; and considering the oscillation and sequential behavior potential of opens. A novel test technique based on controlling the die surface voltage is also descr ...

Keywords: fault simulation, opens, breaks

10 The killer app: how to make millions with ground-breaking software

Ian Clark

June 2000 **ACM SIGAPL APL Quote Quad , Proceedings of the international conference on APL-Berlin-2000 conference APL '00**, Volume 30 Issue 4

Publisher: ACM Press

Full text available: pdf(866.51 KB) Additional Information: full citation, abstract, index terms

I've been a programmer for over 30 years, often at the leading edge, never in a classic IT shop. I've worked with several vendors' mainframes, midis and micros, for big firms, small firms, central government, educational establishments, and for myself; in colleges, universities, laboratories and classrooms; in England, in Europe, and in the USA. I've been involved in some total flops, but in one or two real successes too. I could never tell from the outset which it was going to be. The more I se ...

11 Performance evaluation of connection rerouting schemes for ATM-based wireless networks

Ramachandran Ramjee, Thomas F. La Porta, Jim Kurose, Don Towsley

June 1998 **IEEE/ACM Transactions on Networking (TON)**, Volume 6 Issue 3

Publisher: IEEE Press

Full text available: pdf(181.98 KB) Additional Information: full citation, references, citings, index terms, review

Keywords: ATM, handoffs, wireless networks

12 The Ultimate RISC: A zero-instruction computer

Paul Frenger

February 2000 **ACM SIGPLAN Notices**, Volume 35 Issue 2

Publisher: ACM Press

Full text available: pdf(655.70 KB) Additional Information: full citation, index terms

13 Cell switching versus packet switching in input-queued switches

Yashar Ganjali, Abtin Keshavarzian, Devavrat Shah

August 2005 **IEEE/ACM Transactions on Networking (TON)**, Volume 13 Issue 4

Publisher: IEEE Press

Full text available: pdf(342.41 KB) Additional Information: full citation, abstract, references, index terms

Input Queued (IQ) switches have been well studied in the past two decades by researchers. The main problem concerning IQ switches is scheduling the switching fabric in order to transfer packets from input ports to output ports. Scheduling is relatively easier when all packets are of the same size. However, in practice, packets are of variable length. In the current implementation of switches, variable length packets are segmented into fixed length packets--also knowns as cells--for the purpose o ...

Keywords: cell switching, packet switching, scheduling, variable length packets

14 GPGPU: general purpose computation on graphics hardware

David Luebke, Mark Harris, Jens Krüger, Tim Purcell, Naga Govindaraju, Ian Buck, Cliff Woolley, Aaron Lefohn

August 2004 **Proceedings of the conference on SIGGRAPH 2004 course notes GRAPH '04**

Publisher: ACM Press

Full text available: pdf(63.03 MB) Additional Information: full citation, abstract

The graphics processor (GPU) on today's commodity video cards has evolved into an extremely powerful and flexible processor. The latest graphics architectures provide tremendous memory bandwidth and computational horsepower, with fully programmable vertex and pixel processing units that support vector operations up to full IEEE floating point precision. High level languages have emerged for graphics hardware, making this computational power accessible. Architecturally, GPUs are highly parallel s ...

15 Kizamu: a system for sculpting digital characters

Ronald N. Perry, Sarah F. Frisken

August 2001 **Proceedings of the 28th annual conference on Computer graphics and interactive techniques**

Publisher: ACM Press

Full text available: pdf(4.04 MB) Additional Information: full citation, abstract, references, citings, index terms

This paper presents Kizamu, a computer-based sculpting system for creating digital characters for the entertainment industry. Kizamu incorporates a blend of new algorithms, significant technical advances, and novel user interaction paradigms into a system that is both powerful and unique.

To meet the demands of high-end digital character design, Kizamu addresses three requirements posed to us by a major production studio. First, animators and artists want *digital clay* — a ...

Keywords: ADFs, character design, digital sculpting, distance fields, graphics systems, rendering, triangulation, volume modeling

16 Naltrexone blocks RFR-induced DNA double strand breaks in rat brain cells

Henry Lai, Monserrat Carino, Narendra Singh

November 1997 **Wireless Networks**, Volume 3 Issue 6

Publisher: Kluwer Academic Publishers

Full text available: pdf(401.54 KB) Additional Information: full citation, abstract, references, index terms

Previous research in our laboratory has shown that various effects of radiofrequency electromagnetic radiation (RFR) exposure on the nervous system are mediated by endogenous opioids in the brain. We have also found that acute exposure to RFR induced DNA strand breaks in brain cells of the rat. The present experiment was carried out to investigate whether endogenous opioids are also involved in RFR-induced DNA strand breaks. Rats were treated with the opioid antagonist naltrexone (1 mg/kg, ...

17 Fortran 8X draft

Loren P. Meissner
December 1989 **ACM SIGPLAN Fortran Forum**, Volume 8 Issue 4
Publisher: ACM Press
Full text available: pdf(21.36 MB) Additional Information: full citation, abstract, index terms

Standard Programming Language Fortran. This standard specifies the form and establishes the interpretation of programs expressed in the Fortran language. It consists of the specification of the language Fortran. No subsets are specified in this standard. The previous standard, commonly known as "FORTRAN 77", is entirely contained within this standard, known as "Fortran 8x". Therefore, any standard-conforming FORTRAN 77 program is standard conforming under this standard. New features can b ...

18 The table layout problem

Richard J. Anderson, Sumeet Sobti
June 1999 **Proceedings of the fifteenth annual symposium on Computational geometry**
Publisher: ACM Press
Full text available: pdf(1.15 MB) Additional Information: full citation, references, citings, index terms

19 Reducing signaling traffic in wireless ATM networks through handoff scheme improvement

Anna Hać, Yongcan Zhang
August 2002 **International Journal of Network Management**, Volume 12 Issue 5
Publisher: John Wiley & Sons, Inc.
Full text available: pdf(192.68 KB) Additional Information: full citation, abstract, references, index terms

We propose a new handoff call management scheme which reduces signaling traffic in wireless ATM networks and improves the efficiency of the virtual channel. Chaining followed by a make-break algorithm is a suitable handoff scheme for various situations. In the chaining part of the scheme, a chain routing algorithm is studied and compared with the hop-limiting scheme. When the algorithm is implemented in our scheme, it improves the performance of the existing scheme in call drop rates so as to re ...

20 Fast detection of communication patterns in distributed executions

Thomas Kunz, Michiel F. H. Seuren
November 1997 **Proceedings of the 1997 conference of the Centre for Advanced Studies on Collaborative research**
Publisher: IBM Press
Full text available: pdf(4.21 MB) Additional Information: full citation, abstract, references, index terms

Understanding distributed applications is a tedious and difficult task. Visualizations based on process-time diagrams are often used to obtain a better understanding of the execution of the application. The visualization tool we use is Poet, an event tracer developed at the University of Waterloo. However, these diagrams are often very complex and do not provide the user with the desired overview of the application. In our

experience, such tools display repeated occurrences of non-trivial commun ...

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Terms used **dac make break cell** Found **429** of **173,942**

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1 Transistor level micro-placement and routing for two-dimensional digital VLSI cell synthesis
Michael A. Riepe, Karem A. Sakallah
April 1999 **Proceedings of the 1999 international symposium on Physical design**
Publisher: ACM Press
Full text available: pdf(1.29 MB) Additional Information: full citation, references, citings, index terms

2 CELLERITY: a fully automatic layout synthesis system for standard cell libraries
Mohan Guruswamy, Robert L. Maziasz, Daniel Dulitz, Srilata Raman, Venkat Chiluvuri, Andrea Fernandez, Larry G. Jones
June 1997 **Proceedings of the 34th annual conference on Design automation - Volume 00**
Publisher: ACM Press
Full text available: pdf(104.51 KB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

This paper describes a fully automatic standard-cell layoutsynthesis system, CELLERITY. The system is flexible insupporting a wide variety of process technologies and a range oflibrary template styles. The tool is fully automatic and providesseveral options to the user to customize the layout template. Thetool considers performance and yield and generates dense,design-rule correct layouts. Experimental results indicate that thearea of CELLERITY-generated standard cells is competitive withmanuall ...

3 Accurate and efficient fault simulation of realistic CMOS network breaks
Haluk Konuk, F. Joel Ferguson, Tracy Larrabee
January 1995 **Proceedings of the 32nd ACM/IEEE conference on Design automation**
Publisher: ACM Press
Full text available: pdf(260.64 KB) Additional Information: full citation, references, index terms

4 Analog design space exploration: Efficient description of the design space of analog circuits
Maria del Mar Hershenson
June 2003 **Proceedings of the 40th conference on Design automation**

Publisher: ACM Press
Full text available: pdf(140.90 KB) Additional Information: full citation, abstract, references, index terms

In this paper we present a method for determining the feasible set of analog design problems and we propose an efficient method for their verification. The verification method presented relies on the formulation of the analog circuit design problem as a convex optimization problem in both the design variables and the performance specifications. Since the design is convex not only in the design variables but also in the specification parameters, we observe that the feasible sets are convex and po ...

Keywords: analog, circuits, convex programming, geometric program, optimization, synthesis, verification

5 Coping with buffering: Diffusion-based placement migration

Haoxing Ren, David Z. Pan, Charles J. Alpert, Paul Villarrubia
June 2005 **Proceedings of the 42nd annual conference on Design automation**
Publisher: ACM Press
Full text available: pdf(772.26 KB) Additional Information: full citation, abstract, references, index terms

Placement migration is the movement of cells within an existing placement to address a variety of post-placement design closure issues, such as timing, routing congestion, signal integrity, and heat distribution. To fix a design problem, one would like to perturb the design as little as possible while preserving the integrity of the original placement. This work presents a new diffusion-based placement method based on a discrete approximation to a closedform solution of the continuous diffusion ...

Keywords: diffusion, legalization, placement migration

6 GENAC: an automatic cell synthesis tool

C.-L. Ong, J.-T. Li, C.-Y. Lo
June 1989 **Proceedings of the 26th ACM/IEEE conference on Design automation**
Publisher: ACM Press
Full text available: pdf(628.21 KB) Additional Information: full citation, abstract, references, citings, index terms

We present a solution to the layout problem of cell synthesis, which achieves multiple optimization objectives. In particular, we propose a new hierarchical method for fast and optimal placement of the transistors in a cell. The method minimizes the number of diffusion breaks, and allows a further pursuit of a secondary optimization objective, such as routing channel density. For cells with non-uniform transistor widths, the transistors are folded in such a way as to optimize a cost functio ...

7 Timing issues in placement: Modeling repeaters explicitly within analytical placement

Prashant Saxena, Bill Halpin
June 2004 **Proceedings of the 41st annual conference on Design automation**
Publisher: ACM Press
Full text available: pdf(699.52 KB) Additional Information: full citation, abstract, references, index terms

Recent works have shown that scaling causes the number of repeaters to grow rapidly. We demonstrate that this growth leads to massive placement perturbations that break the convergence of today's interleaved placement and repeater insertion flows. We then present two new force models for repeaters targeted towards analytical placement algorithms. Our experiments demonstrate the effectiveness of our repeater modeling technique in preserving placement convergence (often also accompanied by wire-le ...

Keywords: analytical placement, buffering, force-directed placement, interconnect, placement, repeater insertion, scaling

8 An efficient layout style for 2-metal CMOS leaf cells and their automatic generation

Chi-Yi Hwang, Yung-Ching Hsieh, Youn-Long Lin, Yu-Chin Hsu
June 1991 **Proceedings of the 28th conference on ACM/IEEE design automation**
Publisher: ACM Press
Full text available: pdf(750.81 KB) Additional Information: full citation, references, citings, index terms

9 Global routing considerations in a cell synthesis system

Dwight Hill, Don Shugard
January 1991 **Proceedings of the 27th ACM/IEEE conference on Design automation**
Publisher: ACM Press
Full text available: pdf(601.41 KB) Additional Information: full citation, abstract, references, citings, index terms

Cell synthesis is the process of turning a netlist into an efficient layout without being restricted to a library of predesigned cells or a fixed floorplan. Normally, this job is broken into at least three parts: placement, routing, and detailed cell generation. Each of these tasks are often divided further into a global and a detailed phase. This paper presents cell synthesis system called Sea Of Devices (SOD), with emphasis on its routing phase. In particular, SOD uses a new model for the ...

10 Advances in SAT: Solving difficult SAT instances in the presence of symmetry

Fadi A. Aloul, Arathi Ramani, Igor L. Markov, Karem A. Sakallah
June 2002 **Proceedings of the 39th conference on Design automation**
Publisher: ACM Press
Full text available: pdf(378.79 KB) Additional Information: full citation, abstract, references, citings, index terms

Research in algorithms for Boolean satisfiability and their implementations [23, 6] has recently outpaced benchmarking efforts. Most of the classic DIMACS benchmarks [10] can be solved in seconds on commodity PCs. More recent benchmarks take longer to solve because of their large size, but are still solved in minutes [25]. Yet, small and difficult SAT instances must exist because Boolean satisfiability is NP-complete.We propose an improved construction of symmetry-breaking clauses [9] and apply ...

Keywords: CNF, SAT, difficult, faster, instances, search, speed-up, symmetry

11 Programmable architectures: Dynamic reconfiguration with binary translation: breaking the ILP barrier with software compatibility

Antonio Carlos S. Beck, Luigi Carro
June 2005 **Proceedings of the 42nd annual conference on Design automation**
Publisher: ACM Press
Full text available: pdf(811.10 KB) Additional Information: full citation, abstract, references, index terms

In this paper we present the impact of dynamically translating any sequence of instructions into combinational logic. The proposed approach combines a reconfigurable architecture with a binary translation mechanism, being totally transparent for the software designer. Besides ensuring software compatibility, the technique allows porting the same code for different machines tracking technological evolutions. The target processor is a Java machine able to execute Java bytecodes. Experimental resul ...

Keywords: binary translation, java, power consumption, reconfigurable processors

12 Designing SoCs for yield improvement: Using embedded FPGAs for SoC yield improvement

Miron Abramovici, Charles Stroud, Marty Emmert
June 2002 **Proceedings of the 39th conference on Design automation**
Publisher: ACM Press

Full text available: pdf(200.31 KB) Additional Information: full citation, abstract, references, citings, index terms

In this paper we show that an embedded FPGA core is an ideal host to implement infrastructure IP for yield improvement in a bus-based SoC. We present methods for testing, diagnosing, and repairing embedded FPGAs, for which complete testability is achieved without any area overhead or performance degradation. We show how an FPGA core can provide embedded testers for other cores in the SoC, so that cores designed to be tested with external vectors can be tested with BIST, and the entire SoC can be ...

13 Security as a new dimension in embedded system design: Security as a new dimension in embedded system design

Srivaths Ravi, Paul Kocher, Ruby Lee, Gary McGraw, Anand Raghunathan
June 2004 **Proceedings of the 41st annual conference on Design automation**
Publisher: ACM Press

Full text available: pdf(209.10 KB) Additional Information: full citation, abstract, references, citings, index terms

The growing number of instances of breaches in information security in the last few years has created a compelling case for efforts towards secure electronic systems. Embedded systems, which will be ubiquitously used to capture, store, manipulate, and access data of a sensitive nature, pose several unique and interesting security challenges. Security has been the subject of intensive research in the areas of cryptography, computing, and networking. However, despite these efforts, *security is ...*

***Keywords**: PDAs, architectures, battery life, cryptography, design, design methodologies, digital rights management, embedded systems, performance, security, security processing, security protocols, sensors, software attacks, tamper resistance, trusted computing, viruses*

14 CLIP: integer-programming-based optimal layout synthesis of 2D CMOS cells

Avaneendra Gupta, John P. Hayes
July 2000 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 5 Issue 3
Publisher: ACM Press

Full text available: pdf(371.02 KB) Additional Information: full citation, abstract, references, index terms

A novel technique, CLIP, is presented for the automatic generation of optimal layouts of CMOS cells in the two-dimensional (2D) style. CLIP is based on integer-linear programming (ILP) and solves both the width and height minimization problems for 2D cells. Width minimization is formulated in a precise form that combines all factors influencing the 2D cell width—transistor placement, diffusion sharing, and vertical in ...

Keywords: CMOS networks, circuit clustering, diffusion sharing, integer linear programming, integer programming, layout optimization, leaf cell synthesis, module generation, transistor chains, two-dimensional layout

15 Low power: Low-leakage robust SRAM cell design for sub-100nm technologies

Shengqi Yang, Wayne Wolf, Wenping Wang, N. Vijaykrishnan, Yuan Xie
January 2005 **Proceedings of the 2005 conference on Asia South Pacific design automation ASP-DAC '05**
Publisher: ACM Press
Full text available: pdf(378.11 KB) Additional Information: full citation, abstract, references

A novel low-leakage robust SRAM design for sub-100nm technologies, Hybrid SRAM (HSRAM) cell, is presented in this paper. Leakage power, especially subthreshold leakage and gate leakage, and soft error are challenging the design of SRAM. While these important issues have been separately addressed in previous SRAM designs, there exists no design that simultaneously cuts down leakage power and enhances the resistance to soft error. In this work, we have built the first such SRAM cell, by hybrid of ...

16 System architectures for computer music

John W. Gordon
June 1985 **ACM Computing Surveys (CSUR)**, Volume 17 Issue 2
Publisher: ACM Press
Full text available: pdf(4.61 MB) Additional Information: full citation, abstract, references, citings, index terms, review

Computer music is a relatively new field. While a large proportion of the public is aware of computer music in one form or another, there seems to be a need for a better understanding of its capabilities and limitations in terms of synthesis, performance, and recording hardware. This article addresses that need by surveying and discussing the architecture of existing computer music systems. System requirements vary according to what the system will be used for. Common uses for co ...

17 Architecture 1: Measuring the gap between FPGAs and ASICs

Ian Kuon, Jonathan Rose
February 2006 **Proceedings of the internation symposium on Field programmable gate arrays FPGA'06**
Publisher: ACM Press
Full text available: pdf(193.91 KB) Additional Information: full citation, abstract, references, index terms

This paper presents experimental measurements of the differences between a 90nm CMOS FPGA and 90nm CMOS Standard Cell ASICs in terms of logic density, circuit speed and power consumption. We are motivated to make these measurements to enable system designers to make better informed hoices between these two media and to give insight to FPGA makers on the deficiencies to attack and thereby improve FPGAs. In the paper, we describe the methodology by which the measurements were obtained and we show ...

Keywords: ASIC, FPGA, area comparison, delay comparison, power comparison

18 Formal verification in hardware design: a survey

Christoph Kern, Mark R. Greenstreet
April 1999 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 4 Issue 2
Publisher: ACM Press
Full text available: pdf(411.53 KB) Additional Information: full citation, abstract, references, citings, index terms

In recent years, formal methods have emerged as an alternative approach to ensuring the quality and correctness of hardware designs, overcoming some of the limitations of

traditional validation techniques such as simulation and testing. There are two main aspects to the application of formal methods in a design process: the formal framework used to specify desired properties of a design and the verification techniques and tools used to reason about the relationship between a spec ...

Keywords: case studies, formal methods, formal verification, hardware verification, language containment, model checking, survey, theorem proving

19 A behavioral modeling system for cell compilers

James C. Althoff, Robert D. Shur
June 1985 **Proceedings of the 22nd ACM/IEEE conference on Design automation**
Publisher: ACM Press

Full text available: pdf(668.74 KB) Additional Information: full citation, abstract, references, citings, index terms

In this paper we describe a new behavioral modeling facility that addresses the special demands imposed by a cell compiler-based design system. We present a flexible parameter mechanism that makes it possible to describe cells whose pin configurations vary according to user-supplied parameter values. We also introduce the PRICE timing model which provides for detailed timing descriptions.

20 Poster session 2: Design of a cell library for asynchronous microengines

Gaurav Gulati, Erik Brunvand
April 2005 **Proceedings of the 15th ACM Great Lakes symposium on VLSI**
Publisher: ACM Press

Full text available: pdf(245.53 KB) Additional Information: full citation, abstract, references, index terms

Asynchronous microengines are an attractive alternative to globally synchronous systems for the realization of high performance programmable controllers. However, because of the specific demands of asynchronous signaling, it is not always easy to use existing standard cell libraries to implement asynchronous microengines. In this paper we present the design and evaluation of a CMOS cell set that augments a generic cell library with cells specific to the design of asynchronous microengines. These ...

Keywords: CMOS cell library, asynchronous control, microprogramed control, self-timed systems

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